What is claimed is:

1. A method of forming a one-transistor memory cell, comprising:

(a) forming a dielectric layer over a substrate having a pass-gate formed thereon;

(b) forming an opening in the dielectric layer to expose a portion of the substrate at least adjacent to the pass-gate;

(c) forming a capacitor dielectric layer on sidewalls of the opening in the dielectric layer and on the exposed portion of the substrate; and

(d) forming an electrode layer over the capacitor dielectric layer.

2. The method of claim 1, wherein step (b) further comprises the steps of forming a recess in an isolation region within the substrate, and steps (c) and (d) further comprise forming the capacitor dielectric layer and the electrode layer within the recess of the isolation region.

3. The method of claim 1, wherein steps (c) and (d) comprise:

after step (b), substantially conformally forming the capacitor dielectric layer over the dielectric layer;

forming a planarization layer over the electrode layer; and

removing portions of the planarization layer, the capacitor dielectric layer and the electrode layer directly over the dielectric layer.

4. The method of claim 3, wherein the planarization layer is a dielectric layer.

5. The method of claim 3, wherein the planarization layer is a photoresist layer.

6. The method of claim 5, further comprising the step of removing the photoresist layer within the opening of the dielectric layer after the removing portions step.

7. The method of claim 1, wherein step (b) further comprises using a second dielectric layer formed on a sidewall of the pass-gate as an etching stop layer.

8. The method of claim 1, wherein a space between the pass-gate and the exposed portion of the substrate is from about 400Å to about 1500Å.

9. The method of claim 1, wherein the capacitor dielectric layer comprises a high dielectric constant material layer.

10. The method of claim 9, wherein the capacitor dielectric layer is formed by atomic layer deposition (ALD).

11. The method of claim 9, wherein the electrode layer comprises a metal layer.

12. The method of claim 1 further comprising:

(e) forming a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

(f) forming a doped region within the substrate and adjacent to the pass-gate and the electrode layer.

13. The method of claim 12, wherein the doped region has a dopant concentration lower than that of the S/D region.

14. A method of forming a one-transistor memory cell, comprising:

(a) forming an isolation region within a substrate, a pass-gate over the substrate and a first dielectric layer over the substrate including over the isolation region and the pass-gate;

(b) forming an opening through the first dielectric layer to expose a portion of the substrate at least adjacent to the pass-gate, wherein a second dielectric layer on a sidewall of the pass-gate is used as an etch stop layer and a recess within the isolation region;

(c) forming a capacitor dielectric layer on sidewalls of the opening in the first dielectric layer, at least partially within the recess of the isolation region and on the exposed portion of the substrate;

(d) forming an electrode layer over the capacitor dielectric layer;

(e) forming a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

(f) forming a doped region within the substrate and adjacent to the pass-gate and the electrode layer.

15. The method of claim 14, wherein the steps (c) and (d) comprise:

after step (b), substantially conformally forming the capacitor dielectric layer over the first dielectric layer;

forming a planarization layer over the electrode layer; and

removing portions of the planarization layer, the capacitor dielectric layer and the electrode layer directly over the first dielectric layer.

16. The method of claim 15, wherein the planarization layer is a dielectric layer.

17. The method of claim 15, wherein the planarization layer is a photoresist layer.

18. The method of claim 17 further comprising the step of removing the photoresist layer within the opening of the first dielectric layer after the removing portions step.

19. The method of claim 14, wherein a space between the pass-gate and the exposed portion of the substrate is from about 400Å to about 1500Å.

20. The method of claim 14, wherein the capacitor dielectric layer comprises a high dielectric constant material layer.

21. The method of claim 20, wherein the capacitor dielectric layer is formed by atomic layer deposition (ALD).

22. The method of claim 20, wherein the electrode layer comprises a metal layer.

23. The method of claim 14, wherein the doped region has a dopant concentration lower than that of the S/D region.

24. A one-transistor memory cell, comprising:

a substrate having a pass-gate formed thereover;

a dielectric layer formed over the pass-gate and the substrate and having an opening exposing a portion of substrate adjacent to the pass-gate;

a capacitor dielectric layer on sidewalls of the opening and on the exposed portion of the substrate; and

an electrode layer formed on the capacitor dielectric layer.

25. The one-transistor memory cell of claim 24 further comprising a recess in an isolation region within the substrate, wherein the capacitor dielectric layer is formed at least partially within the recess of the isolation region.

26. The one-transistor memory cell of claim 24, further comprising a second dielectric layer formed on a sidewall of the pass-gate and exposed in the opening within the dielectric layer, wherein the capacitor dielectric layer is formed over the exposed second dielectric layer.

27. The one-transistor memory cell of claim 24, wherein the pass-gate is spaced from the exposed portion of the substrate from about 400Å to about 1500Å.

28. The one-transistor memory cell of claim 24, wherein the capacitor dielectric layer comprises a high dielectric constant material.

29. The one-transistor memory cell of claim 28, wherein the electrode layer comprises a metal layer.

30. The one-transistor memory cell of claim 24 further comprising:

a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

a doped region within the substrate and adjacent to the pass-gate and the capacitor.

31. The one-transistor memory cell of claim 30, wherein the doped region has a dopant concentration lower than that of the S/D region.

32. A dynamic random access memory (DRAM) including a plurality of one-transistor cells, wherein each of the one-transistor cells comprises:

a pass-gate formed over a substrate;

a dielectric layer formed over the pass-gate, the dielectric layer having an opening exposing a portion of the substrate adjacent to the pass-gate;

a capacitor dielectric layer on sidewalls of the opening and on the exposed portion of the substrate; and

an electrode layer formed on the capacitor dielectric layer.

33. The DRAM of claim 32, wherein the one-transistor cell further comprises a recess in an isolation region within the substrate and wherein the capacitor dielectric layer is formed at least partially within the recess of the isolation region.

34. The DRAM of claim 32, wherein a second dielectric layer is formed on a sidewall of the pass-gate and exposed in the opening within the dielectric layer, and the capacitor dielectric layer is formed over the exposed second dielectric layer.

35. The DRAM of claim 32, wherein the capacitor dielectric layer comprises a high dielectric constant material.

36. The DRAM of claim 35, wherein the electrode layer comprises a metal layer.

37. The DRAM of claim 32, wherein the one-transistor cell further comprises:

a source/drain (S/D) region within the substrate and adjacent to the pass-gate; and

a doped region within the substrate and adjacent to the pass-gate and the capacitor.

38. The DRAM of claim 37, wherein the doped region has a dopant concentration lower than that of the S/D region.